REMARKS/ARGUMENTS

The above identified patent application has been amended. Claims 1-3 and 7-10 are currently pending in this application. Claims 1, 2, 7 and 8 have been amended. Claims 4-6 have been previously canceled. In view of the foregoing amendments and remarks that follow, reconsideration and reexamination of the present application is respectfully requested.

The Examiner rejected has Claims 1-3 and 7-10 under 35 U.S.C. 102(b) as being anticipated by Tripathi et al., U.S. Patent 5,974,089 ("Tripathi"). The Examiner has also rejected Claim 10 under 35 U.S.C. §103 as being unpatentable over Tripathi in view of Thompson, U.S. Patent 5,274,375 ("Thompson"). The Applicants respectfully traverse these rejections.

Applicants have amended Claim 1 to call in part for: (emphasis added) ... a sampling means output clock for clocking the discrete-time sampling means to produce an output signal with a lower transition rate being fed back to the means for preliminary noise-shaping to sum with the input signal. Applicants respectfully submit that Tripathi does not disclose or suggest the invention as claimed in Claim 1.

Rather, Tripathi achieves an increased oversampling ratio without suffering the consequences of unacceptably narrow pulse widths by adding pulse qualification logic after a sampling means to eliminate unacceptably narrow pulses. In Tripathi, "comparator stage 310 with a sample frequency f_s receives the output of second integrator stage 306 and transmits the

resulting logic signal to qualification logic 318. Qualification logic 318 ensures that the width of pulses sent to power switching stage are at least some minimum width" (Col. 6, Lines 10-14).

Tripathi further teaches with respect to FIG. 4 that "comparator stage 310 is a 1-bit analog-to-digital (A/D) converter which is triggered on the positive rising edge of the clock signal ... the qualification logic ensures that pulses are sent to the power switching devices at most once every 2 clock cycles (see the qualified output signal) ... the qualification logic operates on the same edge as the A/D converter, i.e., the positive rising edge of the clock signal. This may be achieved by combining the qualification logic and the A/D converter to thereby avoid any additional and undesirable logic delays" (Col. 6, Lines 33-50).

Thus in Tripathi, the qualification logic receives samples from the comparator and ensures that pulses in the waveform are a first time period apart rather than clocking the sampling means with a sampling means output clock to produce an output signal from the sampling means with a lower transition rate as recited in Claim 1 of the present invention.

As such, the Applicants submit that Claim 1 is not anticipated by Tripathi under 35 U.S.C. §102b. Claims 2 and 3 depend from Claim 1. Therefore, dependent Claims 2 and 3 are believed allowable based upon Claim 1.

Applicants have amended Claim 7 to call in part for: (emphasis added) ... a quantizer output clock for clocking the discrete-time sampling circuit to generate an output signal with

a lower transition rate with respect to the predetermined sampling frequency by a predetermined multiple. For the same reasons discussed above, the Applicants respectfully submit that Tripathi does not disclose a quantizer output clock for clocking the discrete-time sampling circuit, and therefore that Claim 7 is also not anticipated by Tripathi under 35 U.S.C. §102b. Claims 8, 9 and 10 depend from Claim 7. As such, dependent Claims 8, 9 and 10 are believed allowable based upon Claim 7.

Accordingly, in view of the above amendments and remarks the Applicants submit that the application is now in condition for allowance. Reconsideration and reexamination of the above Application is hereby requested.

Respectfully submitted,
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